Role of Energy Efficient Sinusoidal PWM Waveform Generator in Cybersecurity

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Abstract: This is an approach to design Energy Efficient Sinusoidal PWM Waveform Generator on FPGA that not only consumes low amount of power but also providing more security. PWM is used for encoding. Hacker dreams to hack the encoding process and use it for their own malicious intention. Our proposed FPGA based PWM Waveform Generator is more secure as hacking of hardware-based encoding by PWM Waveform Generator is almost impossible to break. This is done by varying Ambient Temperature to different level and checking corresponding amount of energy consumed. There is a reduction of Leakage power in the percentage of 60.86 %, 52.17 %, 39.13 % and 21.73 % when we scaled down Ambient Temperature from 50 ^{o}C to 0 ^{o}C, 12.5 ^{o}C, 25 ^{o}C, 37.5 ^{o}C respectively. SPARTAN-6 FPGA family is used to design and implement sinusoidal PWM waveform Generator in our research.

Keywords: Energy Efficient, Sinusoidal PWM Waveform Generator, FPGA, VHDL.

1. Introduction

The basic idea *here* is to generate or synthesize a sinusoidal PWM waveform by passing a digitally generated PWM through a low pass filter. This is technically called Direct to Digital Synthesis (DDS). For the design of energy efficient waveform Generator, we are checking the different level of ambient temperature level. We have analyzed the varying power with the different level of temperature in order to develop the energy efficient sinusoidal PWM waveform generator. For making the energy efficient model, design name is N3 defined the single source input and generate a sinusoidal PWM waveform depending on rising edge clock wave and sel. The whole process of hardware-based design, make it very tough to break into for any expert cyber hacker. That leads us to develop a more secure PWM Waveform Generator. In this work, we have used four different clock frequency 50 MHz, 71.42 MHz, 125 MHz and 500MHz and we have used four different wave pulse frequency 33.33 MHz, 47.61MHz, 83.33MHz and 333.33MHz respectively for the different level of ambient temperature level from 0 ^{o}C to 50 ^{o}C in the step of every 12.5 ^{o}C. Spartan-6 FPGA family is used for simulation and amount of total power consumed is noted down. SPARTAN-6 family is used which has greatest system integration abilities to produce outcome. Some characteristics features about SPARTAN-6 are shown in Fig. 1.

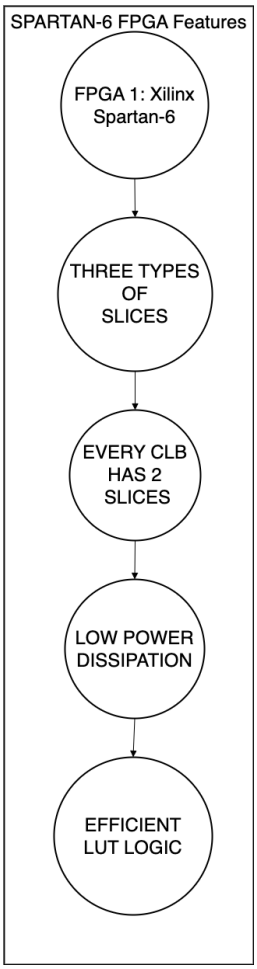

Fig. 1: Some important feature about Spartan-6.

1.1 RTL Schematic

RTL is acronym for Register Transfer Level. RTL of sinusoidal waveform generator is shown in Fig. 2.

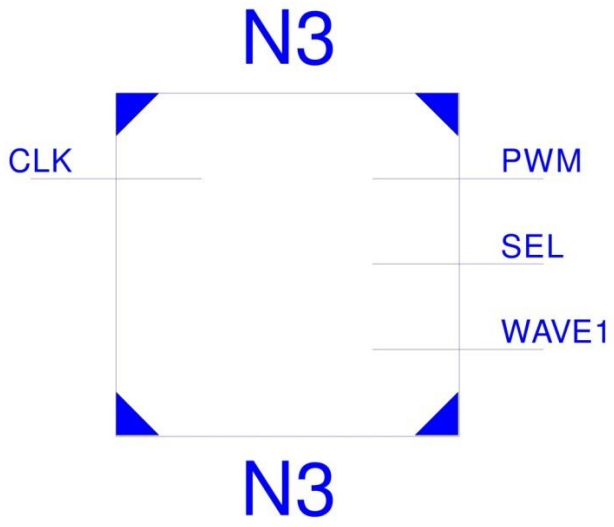

Fig. 2 Basic Architecture of the RTL Schematic.

As shown in the Fig. 2, the RTL has one input clock port and three output port such as PWM, SEL, and WAVE1. RTL Schematics of Sinusoidal PWM Waveform Generator. This block diagram define the external architecture of the N3 model which has total four port one is clock input port and others three are output port which gives the PWM waveform.

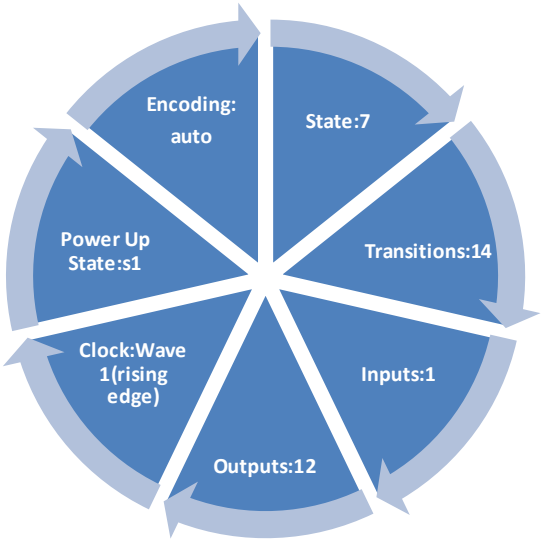

Fig. 3. Initial feature of the synthesizing modal N3 design.

As shown in Fig. 3, model N3 has total of eight HDL synthesizing units. It contains total numbers of States, Transitions, Inputs, Outputs are 7, 14, 1, and 12 respectively. Clocks pulse is raising

edge WAVE1, power Up State is connected to s1, Auto Encoding and LUT Implementation. Fig. 4 illustrates internal architecture of RTL schematics of sinusoidal PWM waveform generator.

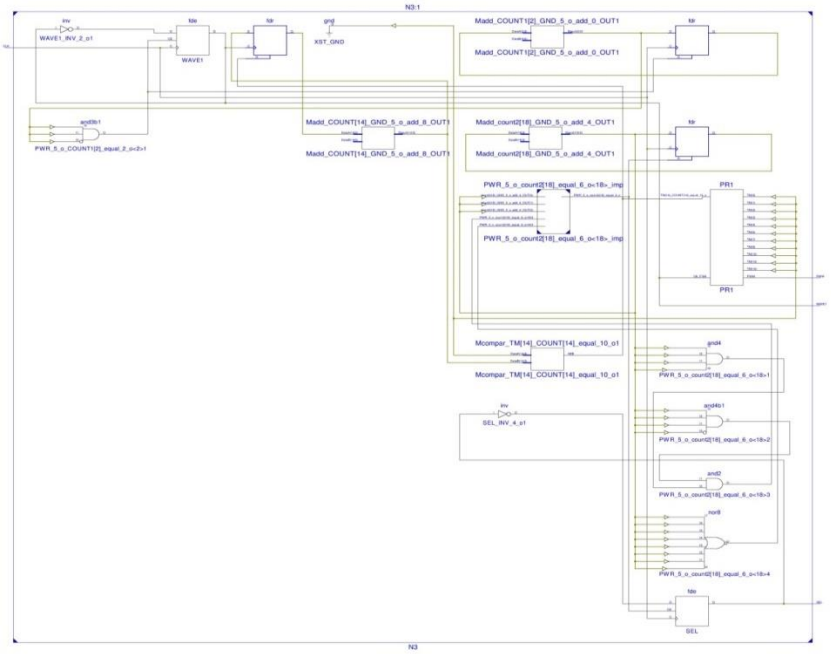

Fig. 4. Internal Architecture of RTL Schematics of Sinusoidal PWM Waveform Generator.

In this type of model, we have HDL synthesis report. HDL Synthesis report has Macro Statistics of components used. This design is using 3 adders, 5 registers, 1 comparator and 1 finite state machine (FSM).

1.2 Technology Schematic

The RTL Schematic describe the technical architecture of the behavior of model N3 design. It has 7 no. of states and corresponding Encoding bits are shown in the Fig. 4 and Table 1. Technology schematic illustrates its actual implemention on FPGA as shown in Fig. 5.

Table 1: State and its Corresponding Encoding Bits of Finite State Machine

State	Encoding
S1	000
S2	001
S3	010
S4	011
S5	100
S6	101
S7	110

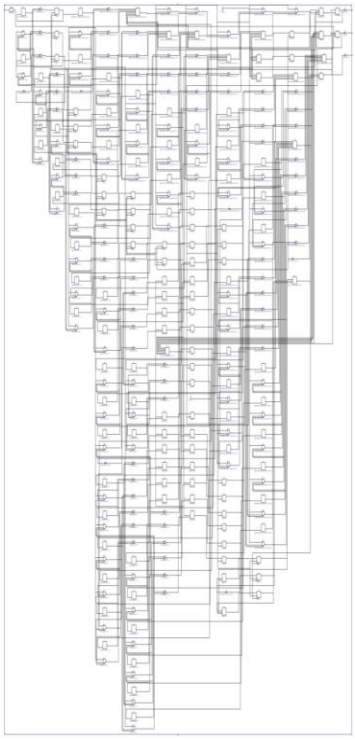

Fig. 5. Technology Schematic of Sinusoidal PWM Waveform Generator.

2. Related Works

In some research work researchers have made energy efficient ALU using Mobile DDR IO standards [1]. In our work, we are making Energy Efficient PWM in place of ALU. We are using Thermal scaling and Frequency scaling in place of Mobile DDR IO standards. Researcher have designed an energy efficient Multiplier using Nikhilam Navatashcaramam Dashatah Vedic technique [2]. In our work, we are making Energy Efficient PWM in place of Multiplier. We are using Thermal scaling and Frequency scaling in place of Nikhilam Navatashcaramam Dashatah Vedic technique. Another researcher has done power dissipation analysis of DES algorithm, implemented on 28nm FPGA [3]. Some researchers have use thermal aware approach in Encoder design and also testing thermal stability by working on different ambient temperatures [4]. We are also using thermal and frequency scaling for the making of design of energy efficient sinusoidal PWM waveform generator. Some other researchers have made Energy Efficient Thermal Aware Image ALU Design on FPGA [5]. One researcher tried to analyze the energy optimization possibility in counter design by selection of energy efficient IO standards [6]. We are design of energy efficient PWM waveform generator. We are using different level of thermal scaling and frequency scaling in place of IO standards. Some other researcher works are using 11 different IO standards from HSTL and LVCMOS family to exploring the feasibility of Vedic multiplier in Data Encryption Algorithm, DSP, reliable system, multimedia and fault tolerant systems [7]. In our work we are making energy efficient PWM in place of multiplier and IO standards. For this work we are using thermal and frequency scaling at different level. Some researcher works have made thermal efficient ALU Design by using six different members of SSTL IOs standard [8]. We are making energy efficient PWM for ALU. For this work, we are using thermal and frequency scaling at different level of ambient temperature and frequency. Researcher have done power analysis of DES algorithm implemented on 28nm FPGA using HTML (H-HSUL, T-TTL, M-MOBILE_DDR, L-LVCMOS) technology [9]. We are using thermal and frequency scaling instead of HTML.

3. Results

Table 2: Power Dissipation when Clock Period is 20ns and Period of Wave Pulse is 30 ns.

Ambient Temperature (in C)	Clocks Power (W)	Logic Power (W)	Signals Power (W)	IOs Power (W)	Leakage Power (W)	Total Power (W)
0	0.002	0.000	0.000	0.008	0.009	0.019
12.5	0.002	0.000	0.000	0.008	0.011	0.021
25	0.002	0.000	0.000	0.008	0.014	0.024
37.5	0.002	0.000	0.000	0.008	0.018	0.028
50	0.002	0.000	0.000	0.008	0.023	0.033

There is a fall of 60.86%, 52.17%, 39.13% and 21.73% in the Leakage Power as the Ambient Temperature is scaled down from 50 (C) to 0, 12.5, 25, 37.5 (C) Degree Celsius Respectively. and the total power goes low by a percentage of 46.66%, 40%, 30%, and 16.66% as the Temperature level is scaled down from 50(C) to 0, 12.5, 25, 37.5 (C) respectively as can be vividly concluded from Table 2. There is no change in Clock Power (W) which is constant value 0.001W and IOs Power(W) which is constant value 0.006W When Ambient Temperature is increasing from 0(C) to 50(C).and here no Logic Power(W) and Signal Power(W) was consumed by circuits when increasing in Ambient Temperature from 0(C) to 50 (C).

Table. 3 Power Dissipation when Clock Period is 14 ns and Period of Wave Pulse is 21 ns.

Ambient Temperature (in C)	Clocks Power (W)	Logic Power (W)	Signals Power (W)	IOs Power (W)	Leakage Power (W)	Total Power (W)
0	0.001	0.000	0.000	0.006	0.009	0.016
12.5	0.001	0.000	0.000	0.006	0.011	0.018
25	0.001	0.000	0.000	0.006	0.014	0.021
37.5	0.001	0.000	0.000	0.006	0.018	0.025
50	0.001	0.000	0.000	0.006	0.023	0.030

There is a fall of 60.86%, 52.17%, 39.13% and 21.73% in the Leakage Power as the Ambient Temperature is scaled down from 50 (C) to 0, 12.5, 25, 37.5 (C) degree Celsius Respectively. and the total power goes low by a percentage of 42.22%, 36.36%, 27.27%, and 15.15% as the Temperature level is scaled down from 50(C) to 0 , 12.5 , 25 , 37.5 (C) respectively as can be vividly concluded from Table 3.There is no change in Clock Power (W) which is constant value 0.002W and IOs Power(W) which is constant value 0.008W When Ambient Temperature is increasing from 0(C) to 50(C).and here no Logic Power(W) and Signal Power(W) was Consumed by circuits when increasing in Ambient Temperature from 0(C) to 50 (C).

Table 4. Power Dissipation when Clock Period is 08 ns and Period of Wave Pulse is 12 ns.

Ambient Temperature (in C)	Clocks Power (W)	Logic Power (W)	Signals Power (W)	IOs Power (W)	Leakage Power (W)	Total Power (W)
0	0.003	0.000	0.000	0.014	0.009	0.026
12.5	0.003	0.000	0.000	0.014	0.011	0.028
25	0.003	0.000	0.000	0.014	0.014	0.031

37.5	0.003	0.000	0.000	0.014	0.018	0.035
50	0.003	0.000	0.000	0.014	0.023	0.040

There is a fall in the total power goes low by a percentage of 35%, 30%, 22.5%, and 12.5% as the Temperature level is scaled down from 50(C) to 0 , 12.5 , 25 , 37.5 (C) respectively as can be vividly concluded from Table 4.There is no change in Clock Power (W) which is constant value 0.003W and IOs Power(W) which is constant value 0.014W When Ambient Temperature is increasing from 0(C) to 50(C).and here no Logic Power(W) and Signal Power(W) was Consumed by circuits when increasing in Ambient Temperature from 0(C) to 50 (C).

Table 5: Power Dissipation when Clock Period is 02 ns and Period of Wave Pulse is 03 ns.

Ambient Temperature (in C)	Clocks Power (W)	Logic Power (W)	Signals Power (W)	IOs Power (W)	Leakage Power (W)	Total Power (W)
0	0.009	0.001	0.000	0.057	0.009	0.077
12.5	0.009	0.001	0.000	0.057	0.011	0.079
25	0.009	0.001	0.000	0.057	0.014	0.082
37.5	0.009	0.001	0.000	0.057	0.018	0.086
50	0.009	0.001	0.000	0.057	0.024	0.092

There is a fall of 62.5%, 54.16%, 41.66% and 25% in the Leakage Power as the Ambient Temperature is scaled down from 50 (C) to 0, 12.5, 25, 37.5 (C) Degree Celsius Respectively. And the total power goes low by a percentage of 16.3%, 14.13%, 10.86%, and 6.52% as the Temperature level is scaled down from 50(C) to 0, 12.5, 25, 37.5 (C) respectively as can be vividly concluded from Table 5. There is no change in Clock Power (W) which is constant value 0.009W and IOs Power(W) which is constant value 0.057W When Ambient Temperature is increasing from 0(C) to 50(C).and There is no change in Logic Power(W) which is constant value 0.001W and no Signal Power(W) was Consumed by circuits when increasing in Ambient Temperature from 0(C) to 50 (C).

4. Conclusion

Reductions in clock, logic, IOs, leakage and total power are noted down successfully. It is very clear from tables that at higher value of ambient temperature more power is consumed and vice versa. This will help in designing low power sinusoidal PWM waveform generator for efficient output. Spartan-6 gives low power readings and so is efficient for designing of not only sinusoidal PWM waveform generator but various electronic designs. The frequency range used from50M Hz to 500MHz for clock pulse and 33.33 MHz to 333.33MHz for wave pulse. For this frequency range the value of clock and IOs power remains same and logic and signal power is negligible for different level of changing the ambient temperature but due to leakage there is noticeable difference in total power consumed. Work is done in order to have an efficient design.

5. Future Scope

These results can be used in future for making efficient sinusoidal PWM waveform generator on FPGA. The work has been done on various frequency at different level of ambient temperature. It

is important to make this useful device efficient and a lot of work can be done in this field further. We can also use different FPGA families like automotive Artix-7, automotive coolrunner-2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan-3A, automotive Spartan-3E, automotive Spartan-6, Spartan-3, Spartan-3E. It is important to make this useful device efficient and a lot of work can be done in this field further.

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